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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,959	07/30/2001	Tomoyuki Taguchi	JP920000005US1 (14606)	9354

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EXAMINER

CHAN, EMILY Y

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 02/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/917,959

Applicant(s)

TAGUCHI, TOMOYUKI

Examiner

emily y chan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to Priority Doc filed on 30 July 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Drawings***

Figures 8-10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be abeyance.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

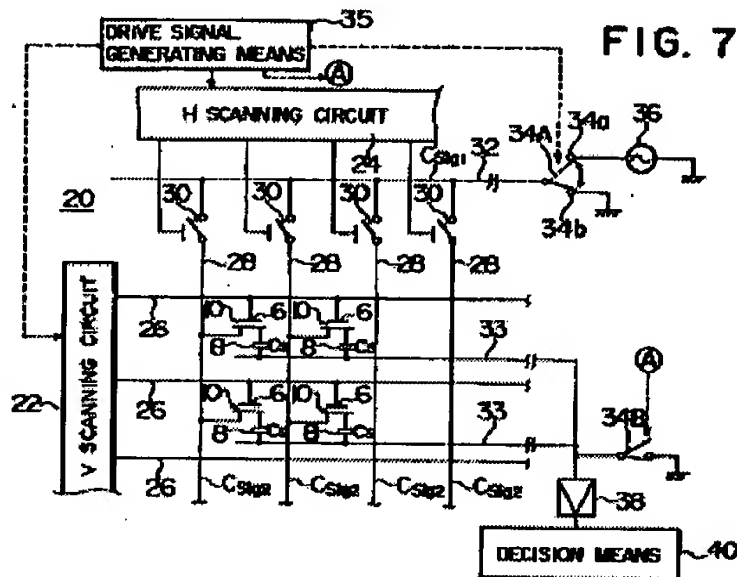
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

. Claims 1-2, and 7-14 are rejected under 35 U.S.C. 102 (b) as being anticipated by Suzuki et al ('030).

With respect claims 1-2 and 13-14, Suzuki et al ('030) disclose an inspection method and device for an array substrate as claimed (see fig 7) below, in which the array substrate comprises: a substrate (5); a plurality of gate lines (26); a plurality of signal lines (28); a plurality of storage capacitor lines (33); a plurality of switching elements (6) electrically connected respectively to the a plurality of gate lines (26) ; a plurality of switching elements (30) electrically connected respectively to the a plurality of signal lines (28); and a plurality of storage capacitors (8) electrically connected respectively to the plurality of storage capacitor lines (33) and to the plurality of

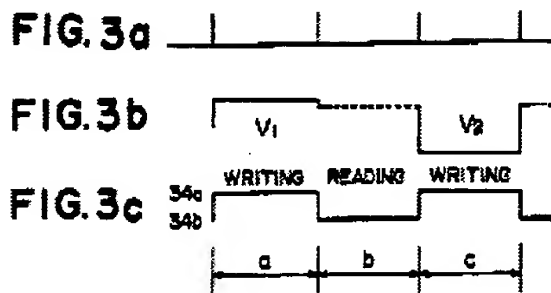
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switching elements (6) (see 5, lines 30-35). Suzuki et al ('030) expressly teach (see col. 7, lines 12-20 and col. 11, lines 1-5) that:



- (1) Applying voltage signals (V2) from the plurality of storage capacitor lines (33) to the plurality of storage capacitors (8);
- (2) Applying voltage signal (V1) from the plurality of signal lines (28) to the plurality of storage capacitors (8) via a plurality of switching elements (30); and
- (3) Measuring quantities of charge stored in the storage capacitors (8) by a circuit (40) based on potential difference between the two voltage signal (V1 and V2) (see col. 7, lines 12-20, 35-38 and col. 11, lines 1-5).

Although Suzuki et al ('030) does not explicitly state in the specification that the pulse signal as claimed, however, it is seen from Fig 3 of Suzuki et al ('030) below that the voltage signal is a pulse signal. Therefore, Suzuki et al ('030) anticipate the claimed method and device.



With respect claims 7 and 9, Suzuki et al ('030) teach that the quantities of charges stored in one storage capacitors (8) connected to storage capacitor lines (33) is measured (see col. 3, lines 25-27).

With respect to claims 8, 10, Suzuki et al ('030) teach that the measuring of the quantity of charges stored in one storage capacitors (8) is performed for all of storage capacitor lines (33) See col. 3, lines 5-17 and 28-31).

With respect to claims 11-12, Suzuki et al ('030) teach that wherein in the measuring step, the quantities of charges stored in the plurality of storage capacitors (8) connected to the signal lines (28) via the plurality of switching elements (30) are measured (see col.7 and Fig 2).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Tomitam ('061).

With respect to claim 3, Suzuki et al ('030) does not teach that the **pulse signals** applied from said plurality of storage capacitor lines to said plurality of storage capacitors and the pulse signals applied from said plurality of signal lines to said plurality of storage capacitors via said plurality of switching elements are **simultaneously** applied to said plurality of storage capacitors.

Tomitam ('061) discloses a testing method for substrate of active matrix display panel and expressly teaches that a pulse signal 20V applied from a plurality of storage capacitor lines (52) to plurality of storage capacitors (61) and a pulse signal 5V from a plurality of signal lines (X) to plurality of storage capacitors (61) are simultaneously applied to the plurality of storage capacitors (61) (see col. 9, lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention at the time the invention was made to incorporate the teaching of Tomitam ('061)' test method of a substrate into Suzuki et al ('030)'s device for the purpose of locating or inspecting a defect pixel in the array substrate to improve the product yield and a reliability as disclosed by Tomitam ('061) (see col. 2, lines 20-23 and lines 65-67).

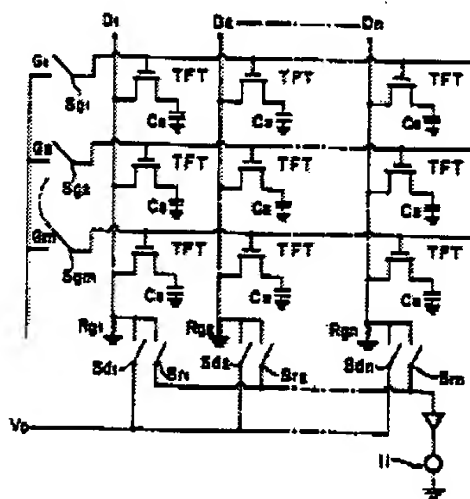
With respect to claims 4-6, Suzuki et al ('030) does not teach that the **pulse signal** has different rising times; however, Tomitam ('061) teach the use of two pulse signals (20V, 5V). Because Tomitam ('061) does not specify the rising times of the two pulse signals are the same, therefore, it would have been obvious to one of ordinary skill in the art that the rising times are different.

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Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Takahashi et al ('300).

Suzuki et al ('030) does not teach that the circuit (40) for measuring the quantities of charges stored in said storage capacitors is connected to the signal lines.

Takahashi et al ('300) disclose a method and apparatus for testing TFT-LCD and expressly teach a circuit (waveform analyzer 11) for measuring the quantities of discharge released from the storage capacitor (see Fig 10 below) is connected to signal lines (D1...Dn) through relays (Sr1...Srn).

**FIG. 10**

It would have been obvious to one of ordinary skill in the art at the time the invention as made to incorporate the teaching of Takahashi et al ('300)' measuring circuit connected to the signal lines into Suzuki et al ('030)'s device, because by using a relay, whether or not the TFTs corresponding to the individual pixels are properly connected can be determined efficiently as disclose by Takahashi et al ('300) (see col. 6, lines 25-30).

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**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily y Chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached on 7033081233. The fax phone numbers for the organization where this application or proceeding is assigned are 7033085841 for regular communications and 7033085841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

  
KAMAND CUNEO  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

EC  
February 11, 2003